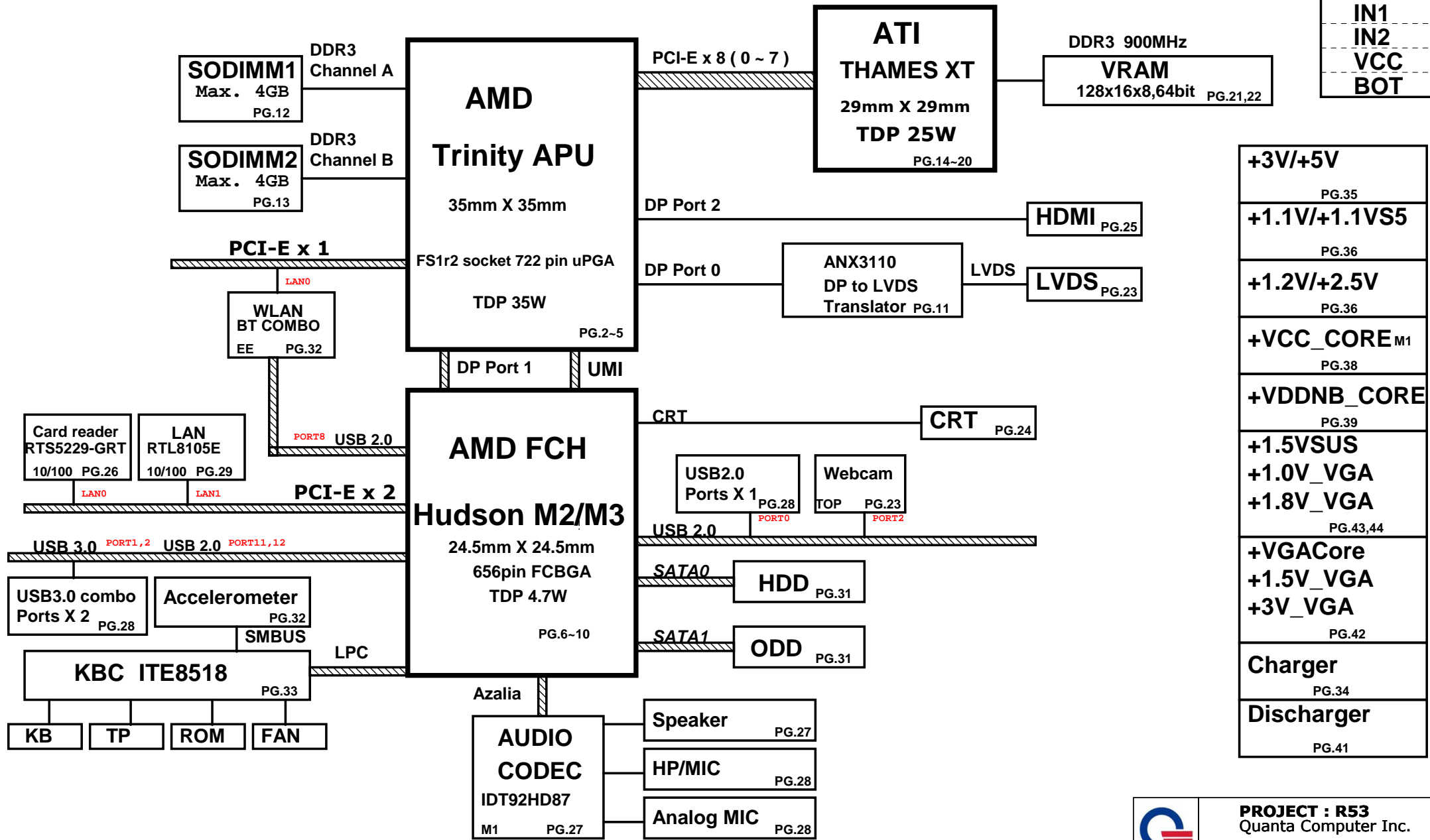


R53 AMD Comal UMA/Muxless SYSTEM DIAGRAM

Stackup

TOP
GND
IN1
IN2
VCC
BOT



+3V/+5V
PG.35
+1.1V/+1.1VS5
PG.36
+1.2V/+2.5V
PG.36
+VCC_CORE M1
PG.38
+VDDNB_CORE
PG.39
+1.5VSUS
+1.0V_VGA
+1.8V_VGA
PG.43,44
+VGACore
+1.5V_VGA
+3V_VGA
PG.42
Charger
PG.34
Discharger
PG.41



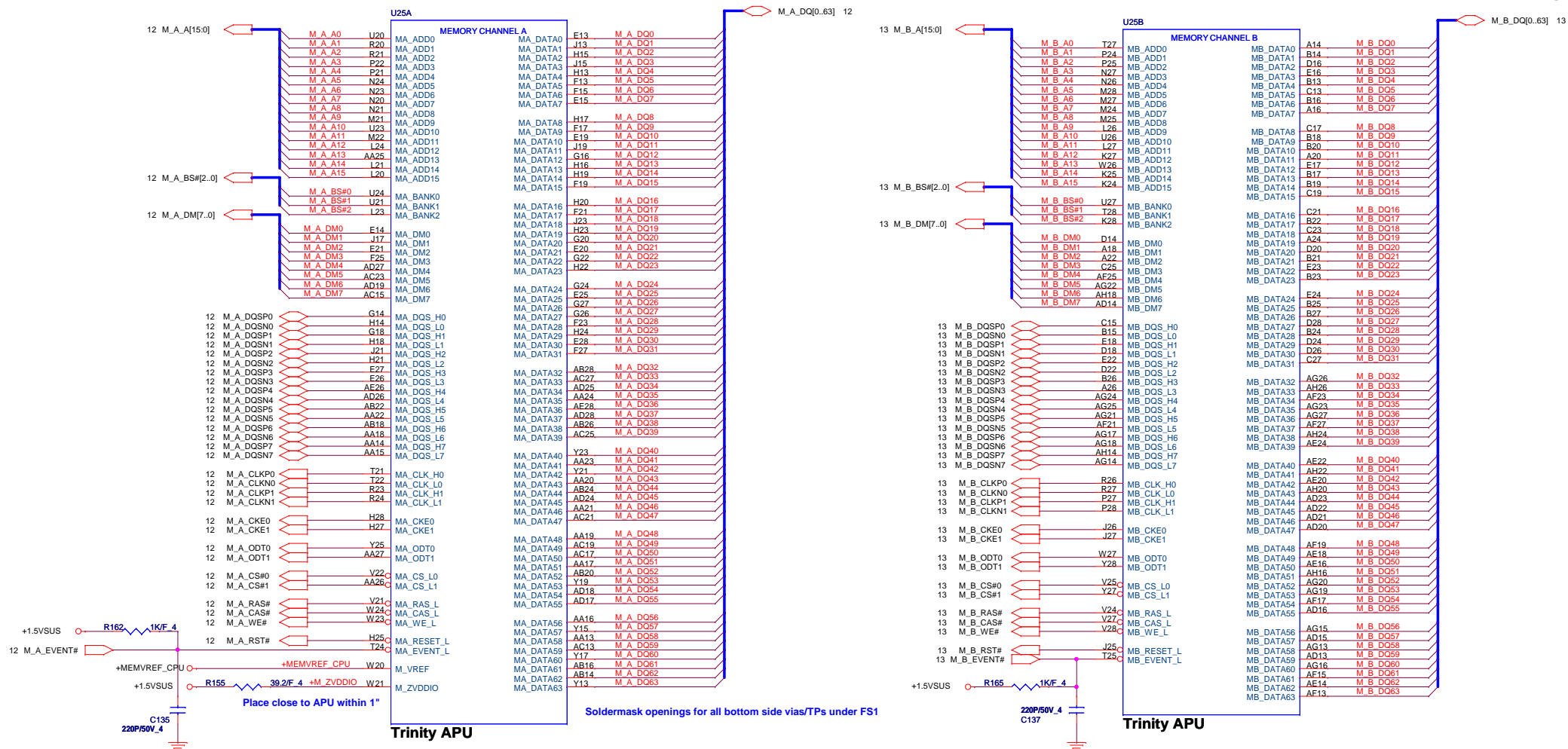
VID Override Circuit



		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

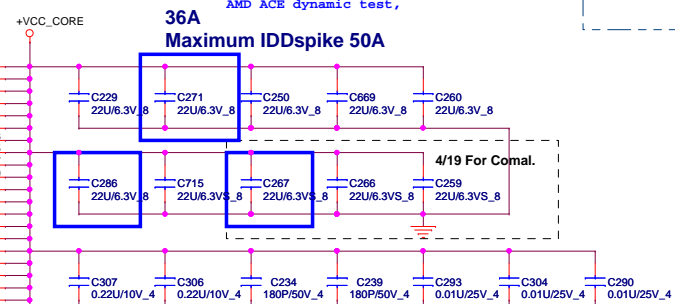
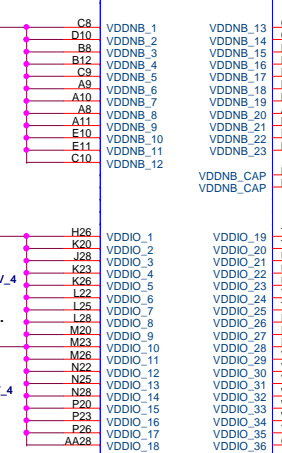
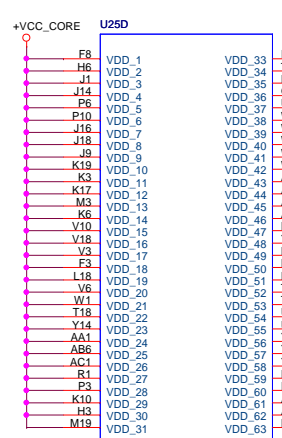
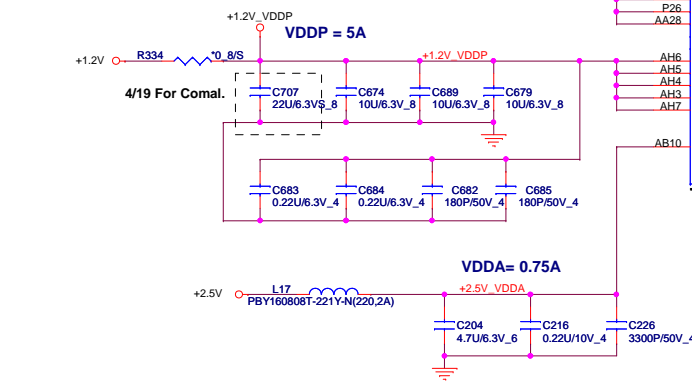
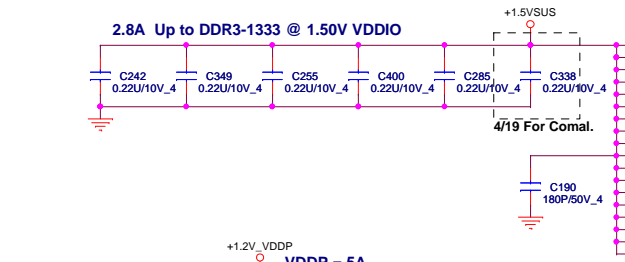
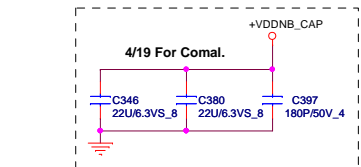
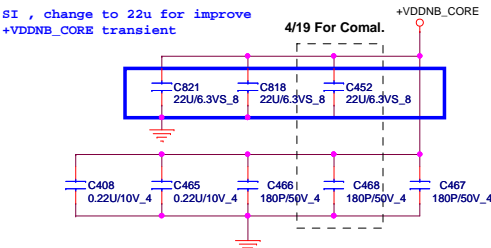


Size Custom	Document Number Llano PCIE/UMI/GPP	Rev 1A
Date: Monday, November 14, 2011		Sheet 2 of 44

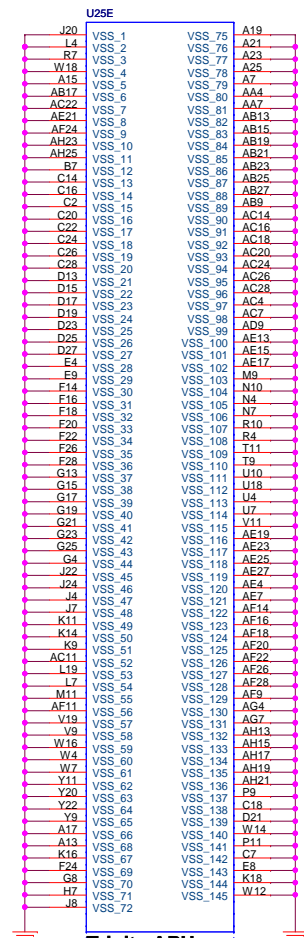
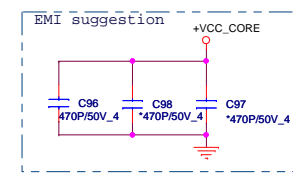
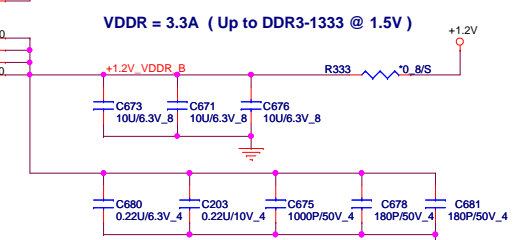
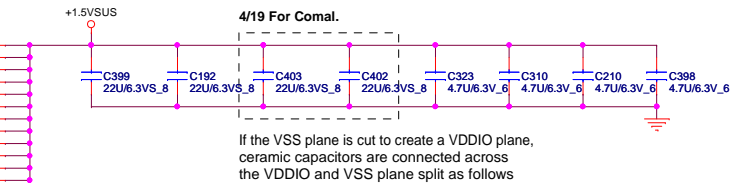
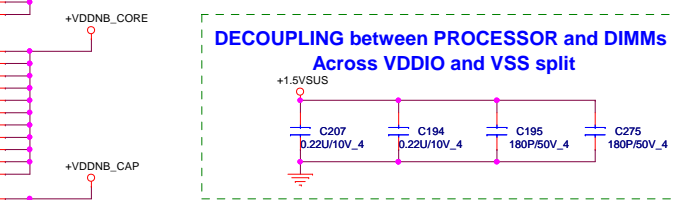


Pin Name	Net Name	Voltage
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

SI , change to 22u for improve
+VDDNB_CORE transient



25A
Maximum IDDNBspike 33A

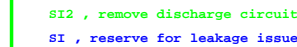


Trinity APU

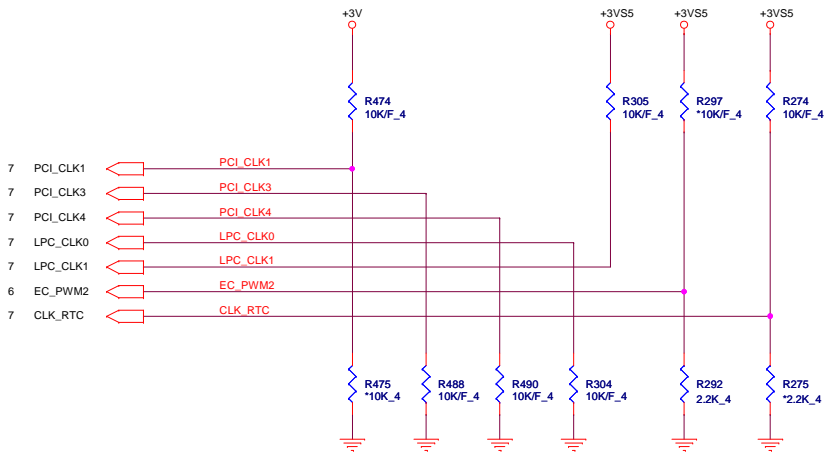
	PROJECT : R53		
	Quanta Computer Inc.		
	Size Custom	Document Number Llano POWER/GND	Rev 1A
	Date: Friday, November 11, 2011	Sheet 5	of 44







OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

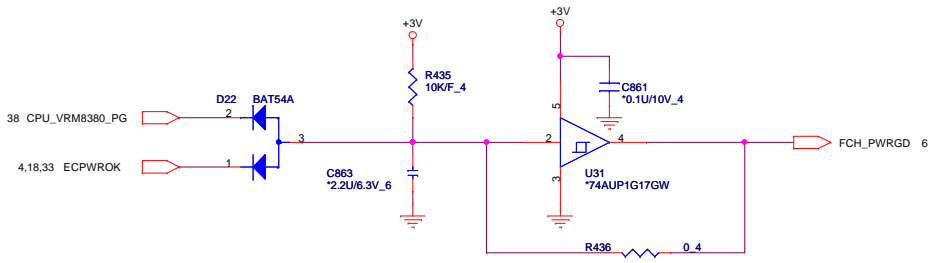
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



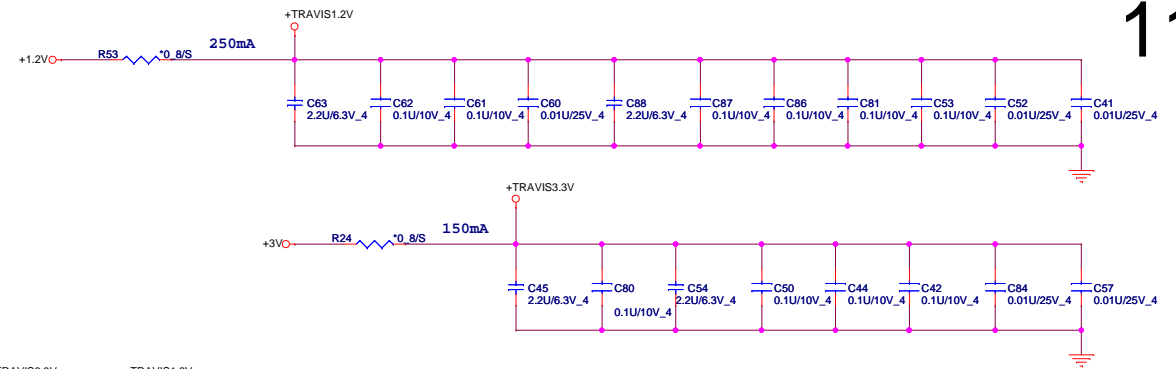
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

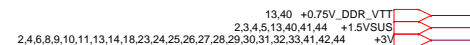
FCH_PWRGD

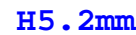


PROJECT : R53
Quanta Computer Inc.

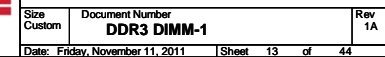
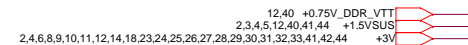
Size Custom	Document Number Hudson-M3 STRAP/PWRGD	Rev 1A
Date: Friday, November 11, 2011	Sheet 10	of 44

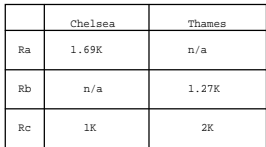






SI , change to 1000P
to meet ref design





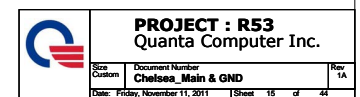
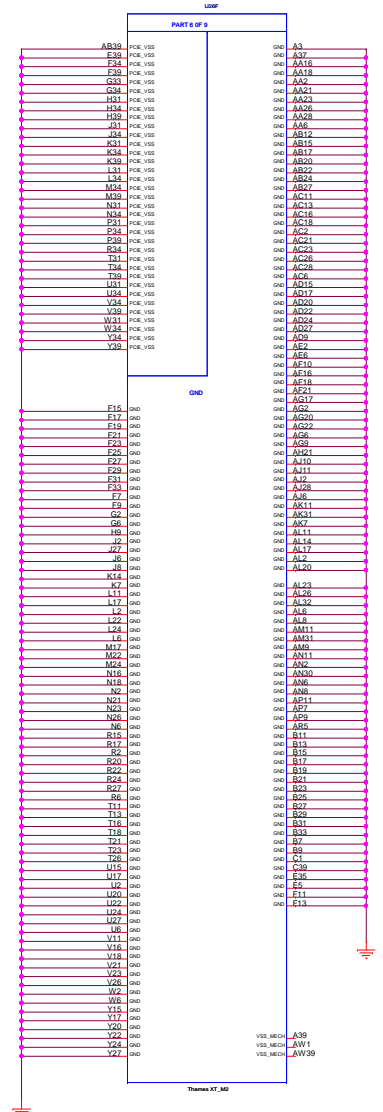
	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

16,18,19,44	+1.0V_VGA		+1.0V_VGA
15,16,18,19,43	+1.8V_VGA		+1.8V_VGA

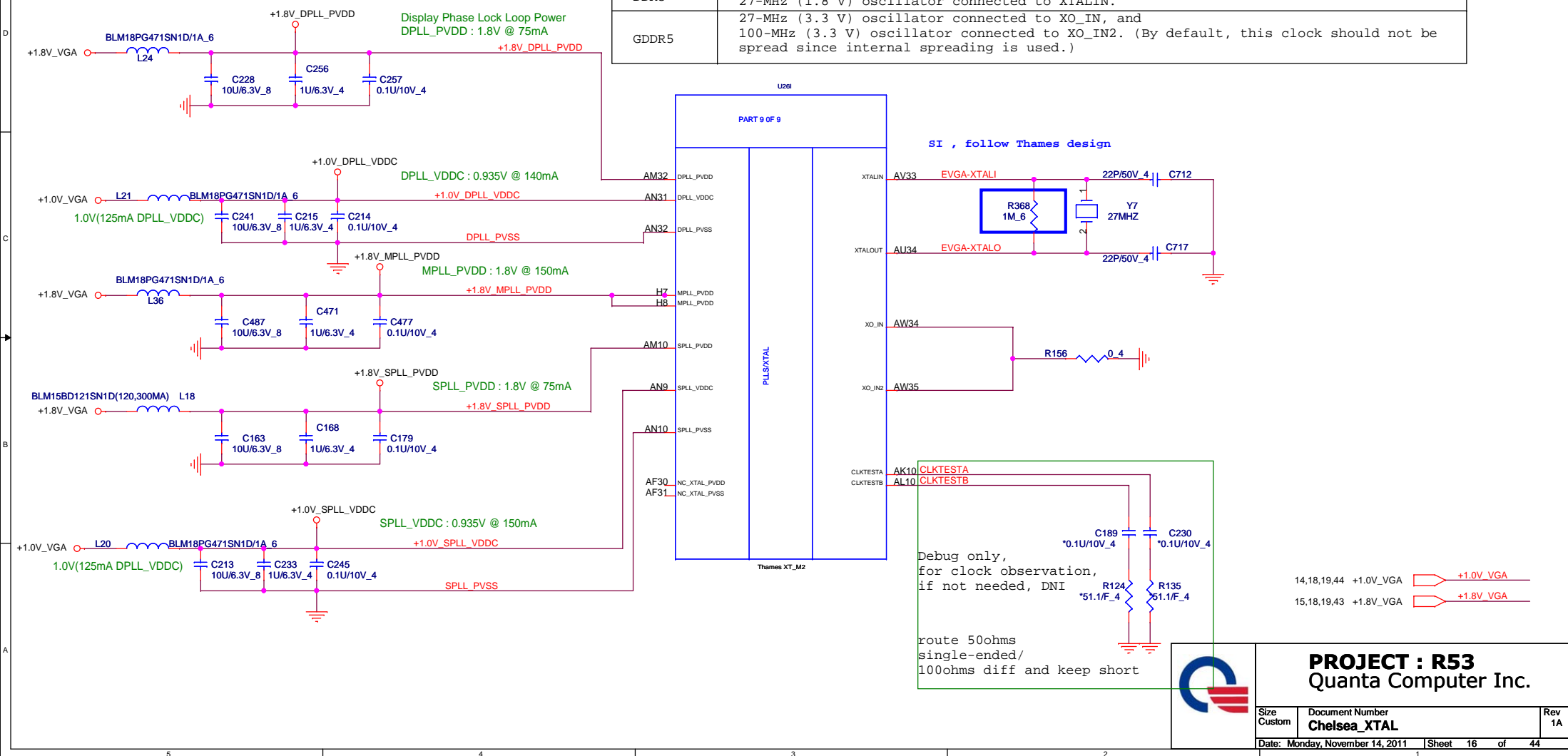
PROJECT : R53
Quanta Computer Inc.

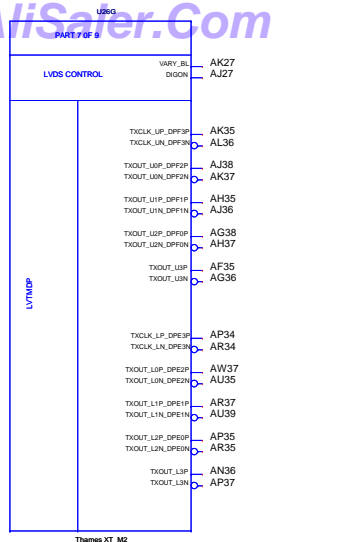
Size Custom	Document Number Chelsea SPIE Interface	Rev 1A
Date: November 14, 2011 Sheet: 14 of 44		

	GPIO16	GPIO20	GPIO15	
Thames-XT	FWRCNTL 2	FWRCNTL 1	FWRCNTL 0	VGA CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V



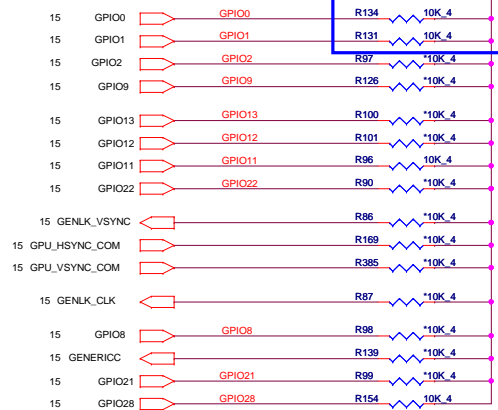
Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)





SI, default setting should be PU from AMD SCH review result

+3V_DELAY



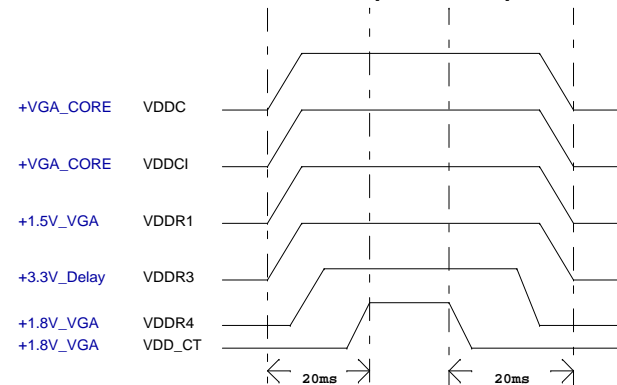
Memory Aperture size

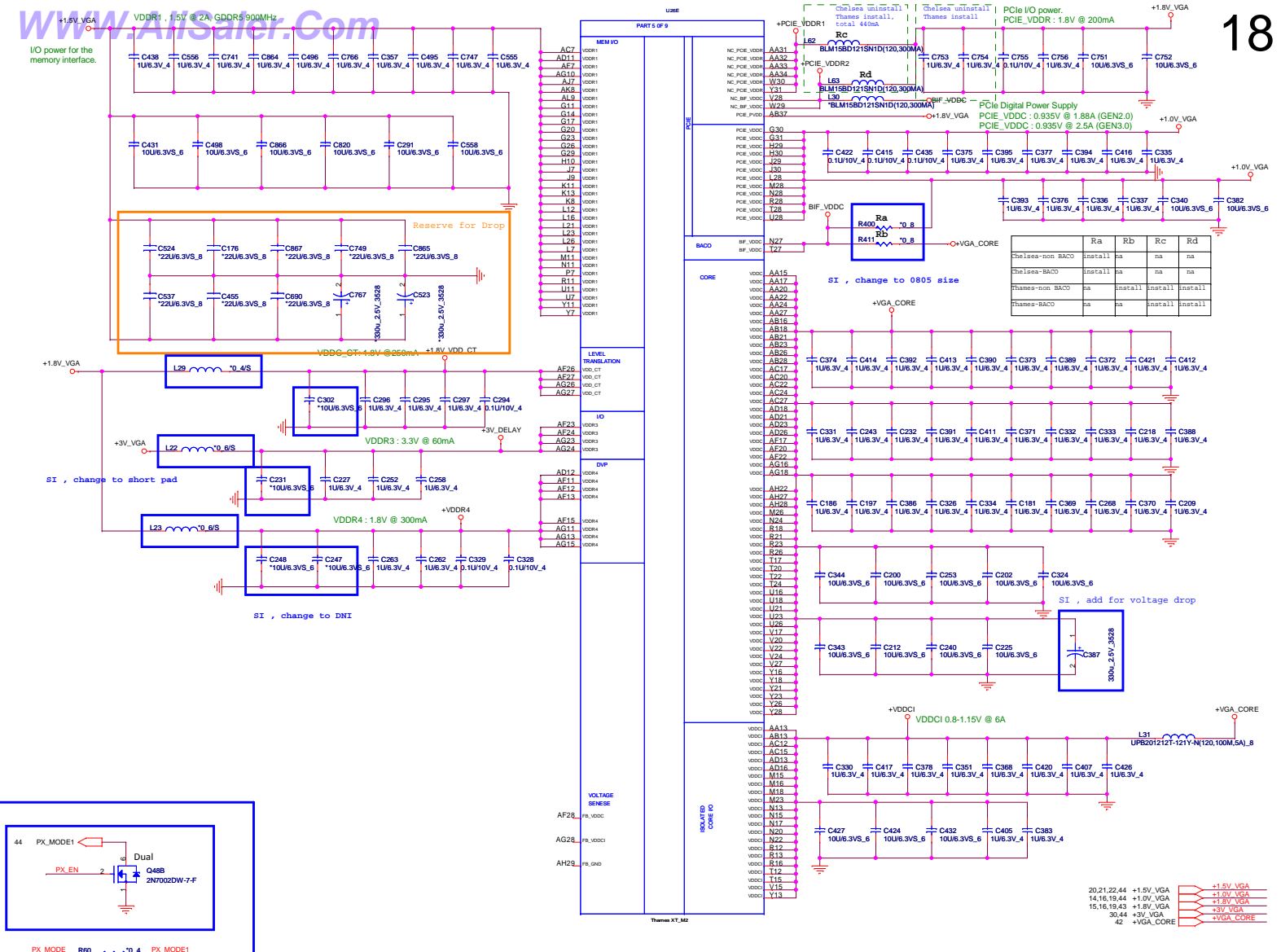
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

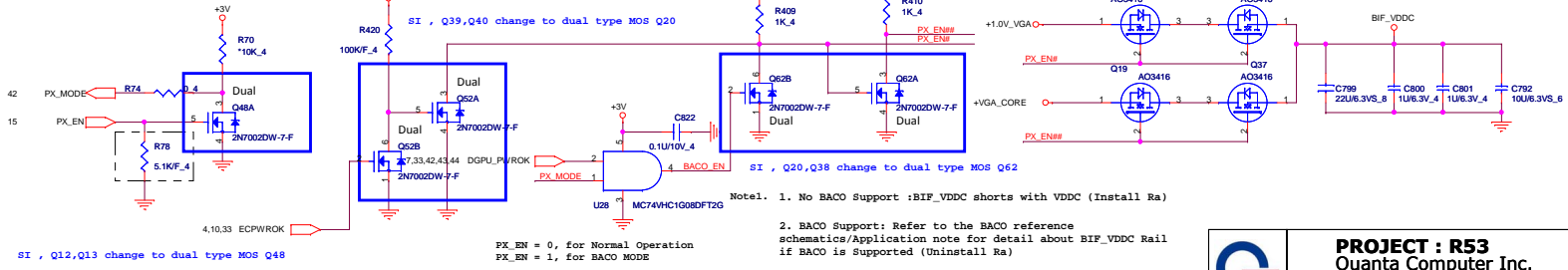
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS. NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 2Mbit M25P10A (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Power Up/Down Sequence



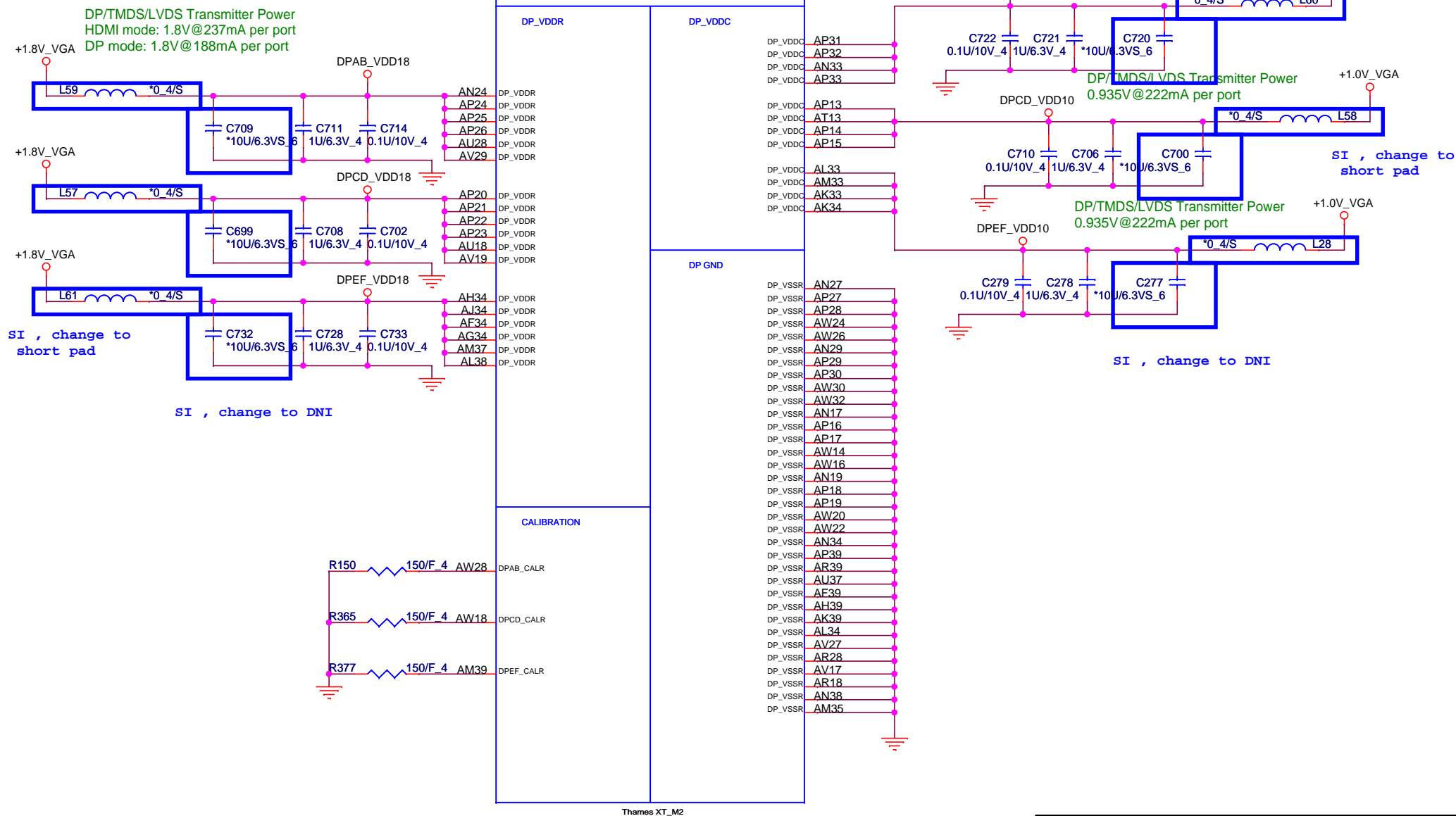


Support BACO Mode



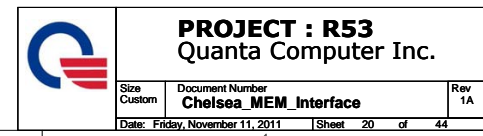
For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

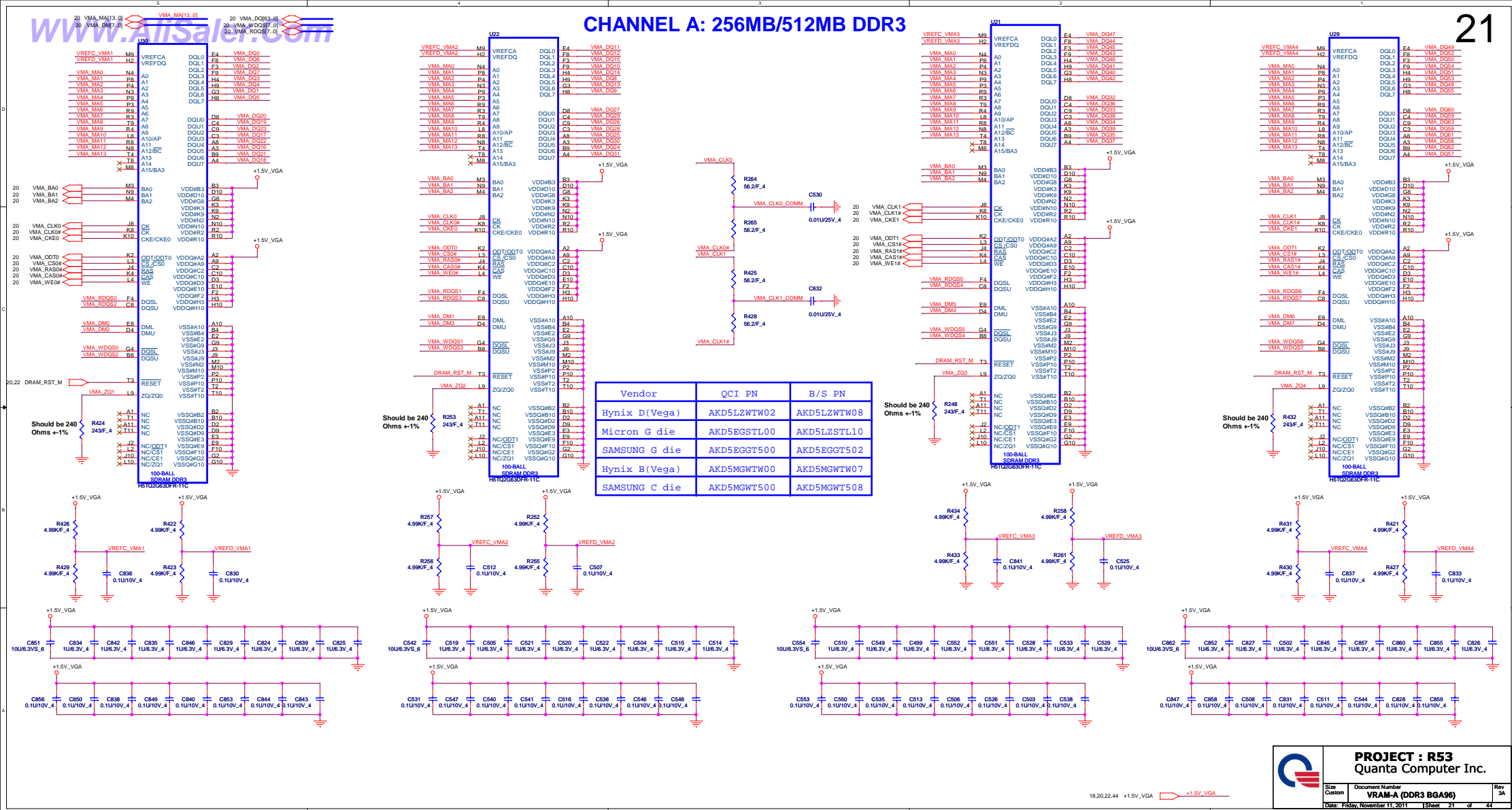


PROJECT : R53
Quanta Computer Inc.

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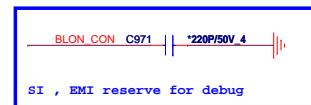
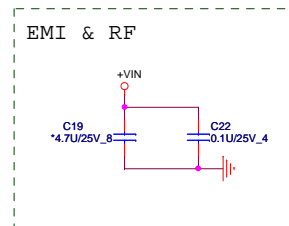
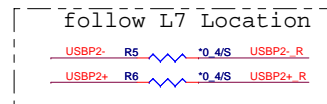
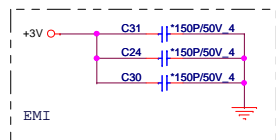
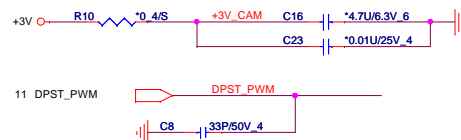
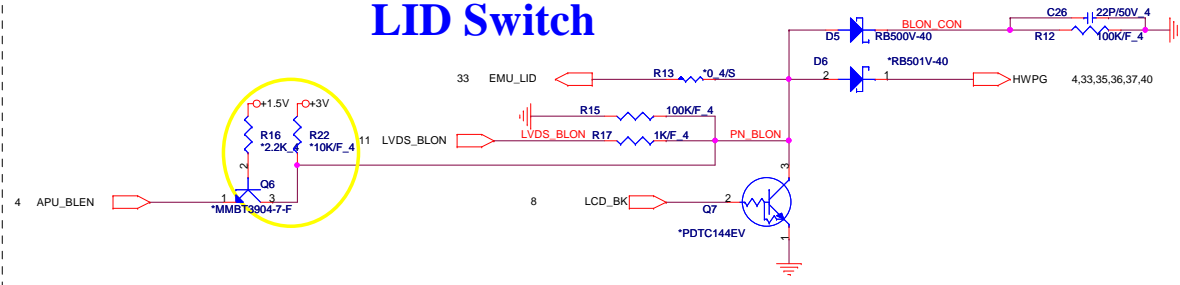


CHANNEL A: 256MB/512MB DDR3

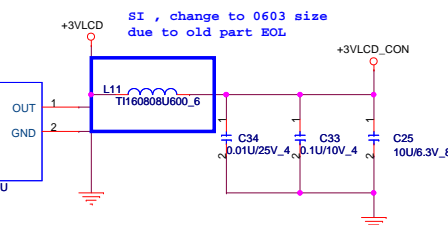
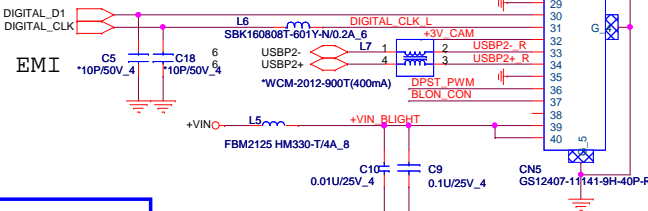
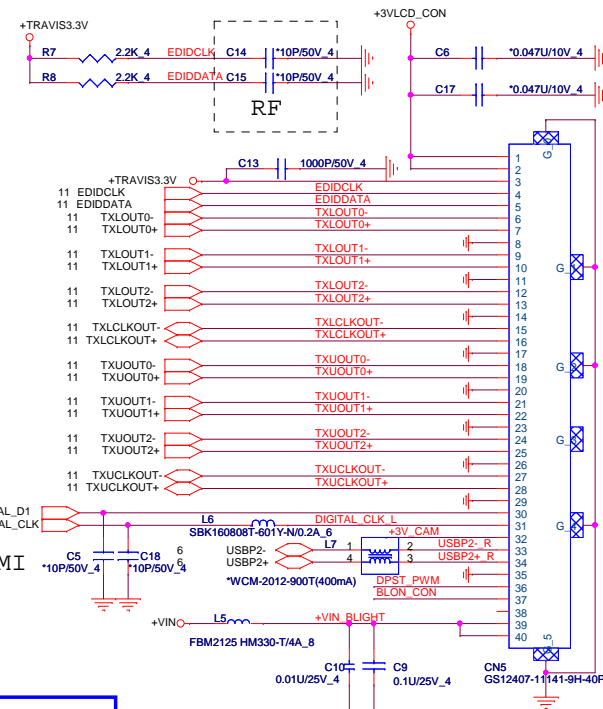
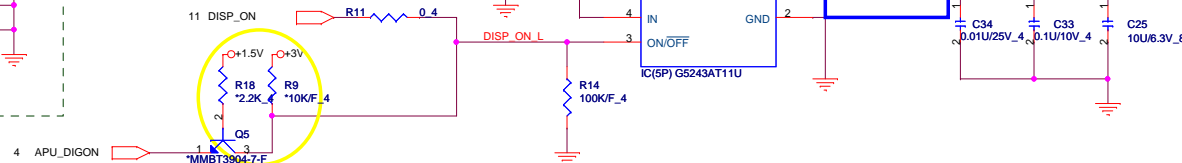
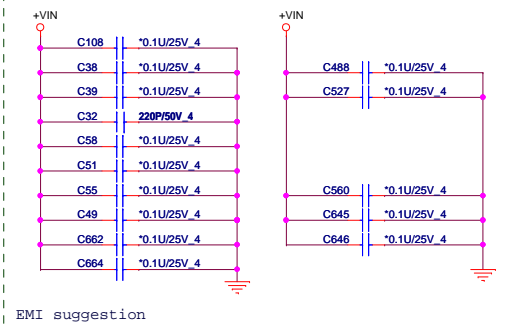




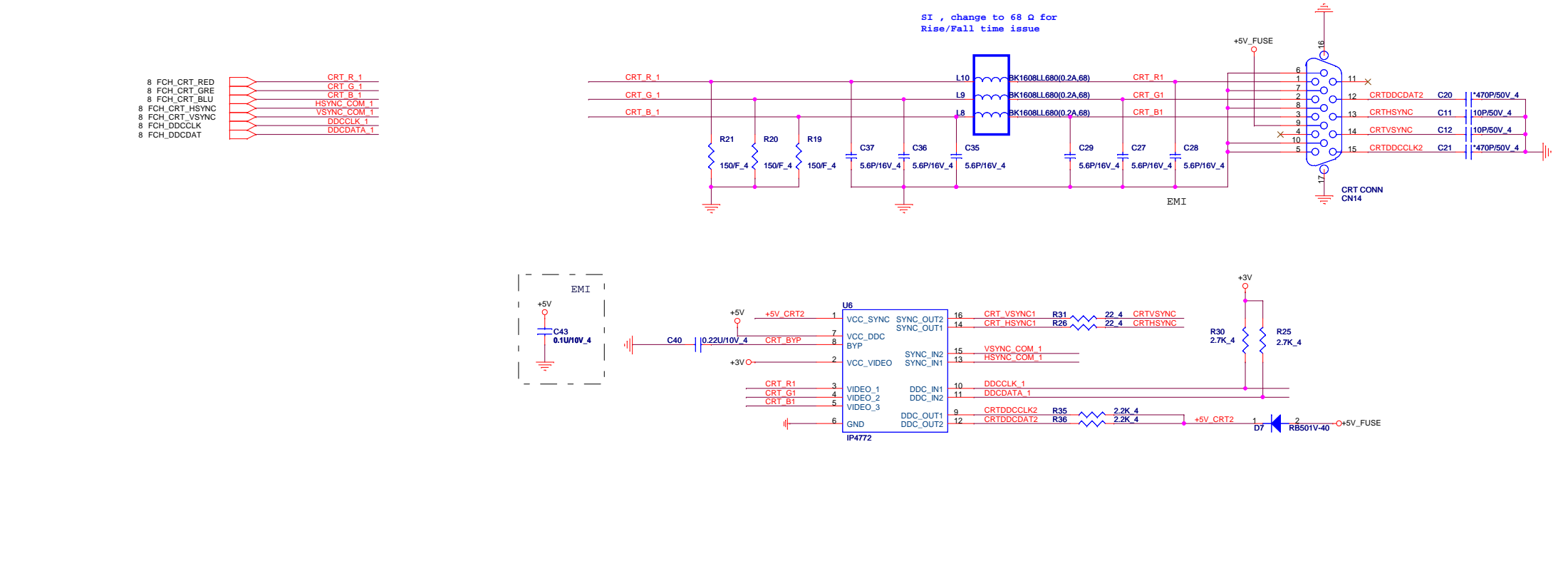
LID Switch



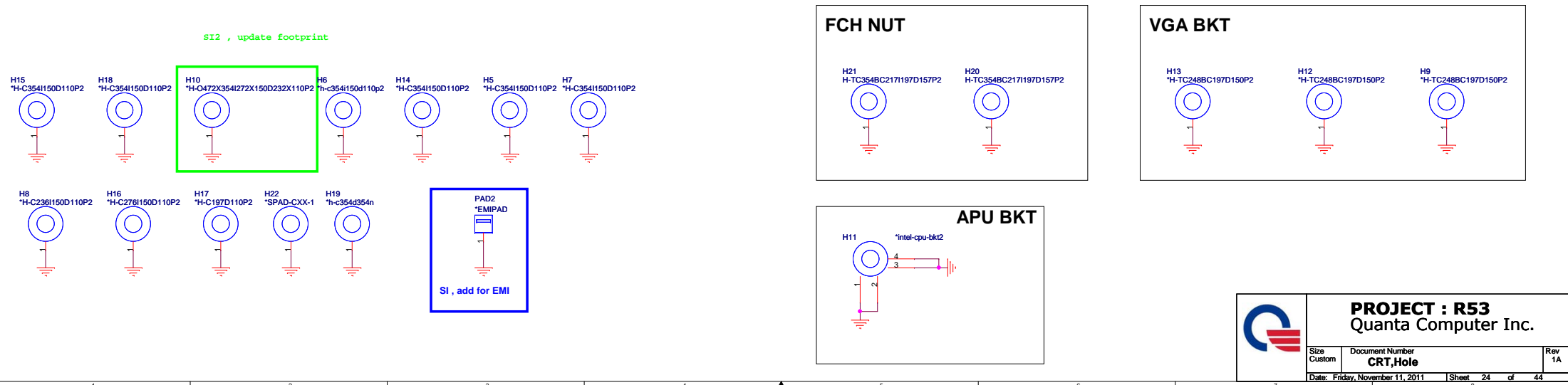
Coupling CAP.



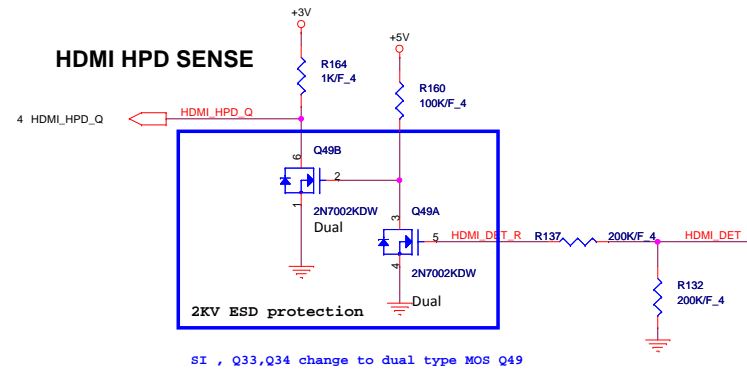
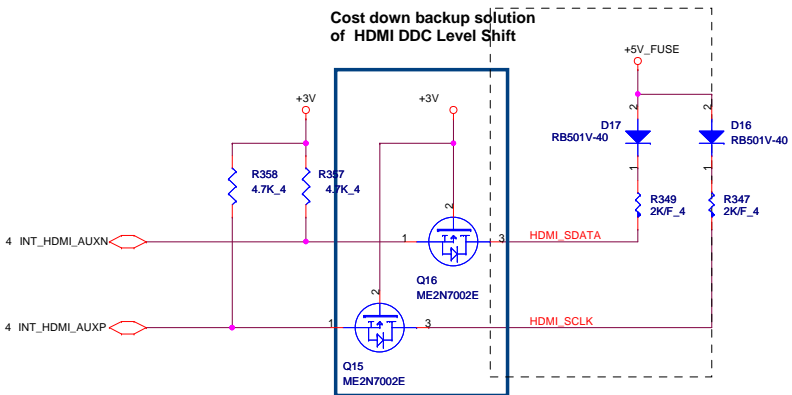
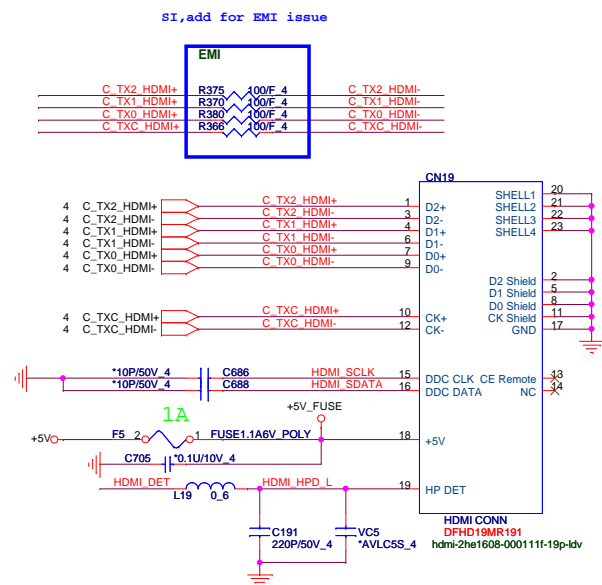
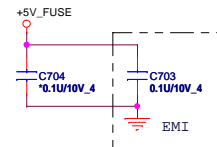
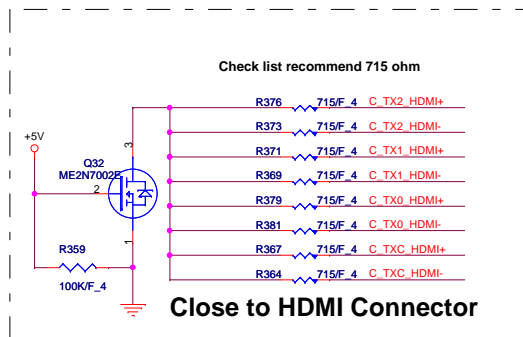
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Size Custom	Document Number LCD CONN/LID/CAM	Rev 1A	
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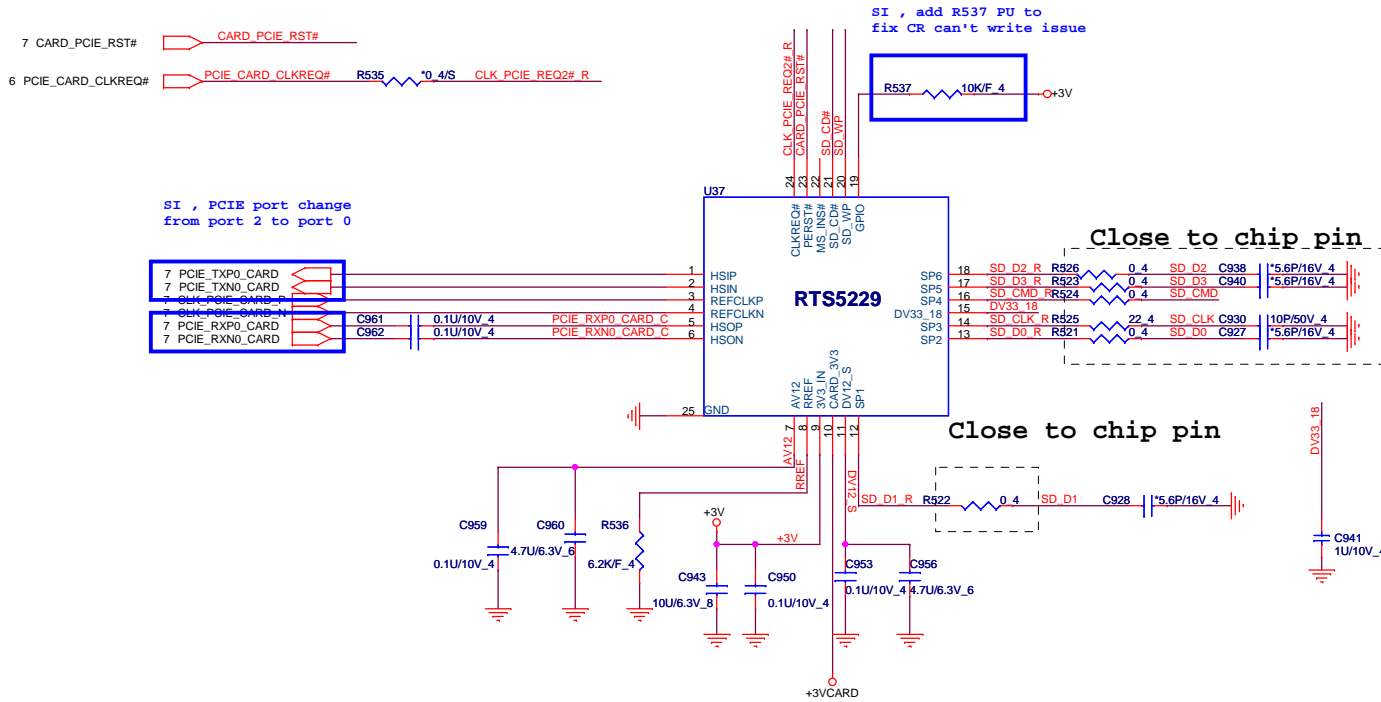


HOLE

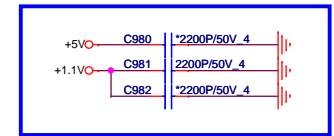


	PROJECT : R53 Quanta Computer Inc.	
	Size Custom	Document Number CRT,Hole
	Date: Friday, November 11, 2011	Sheet 24 of 44



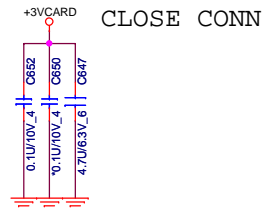
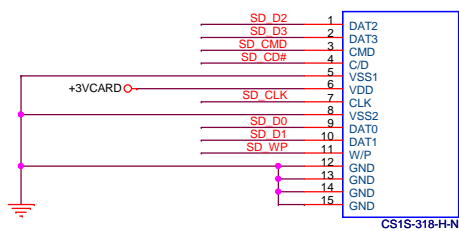


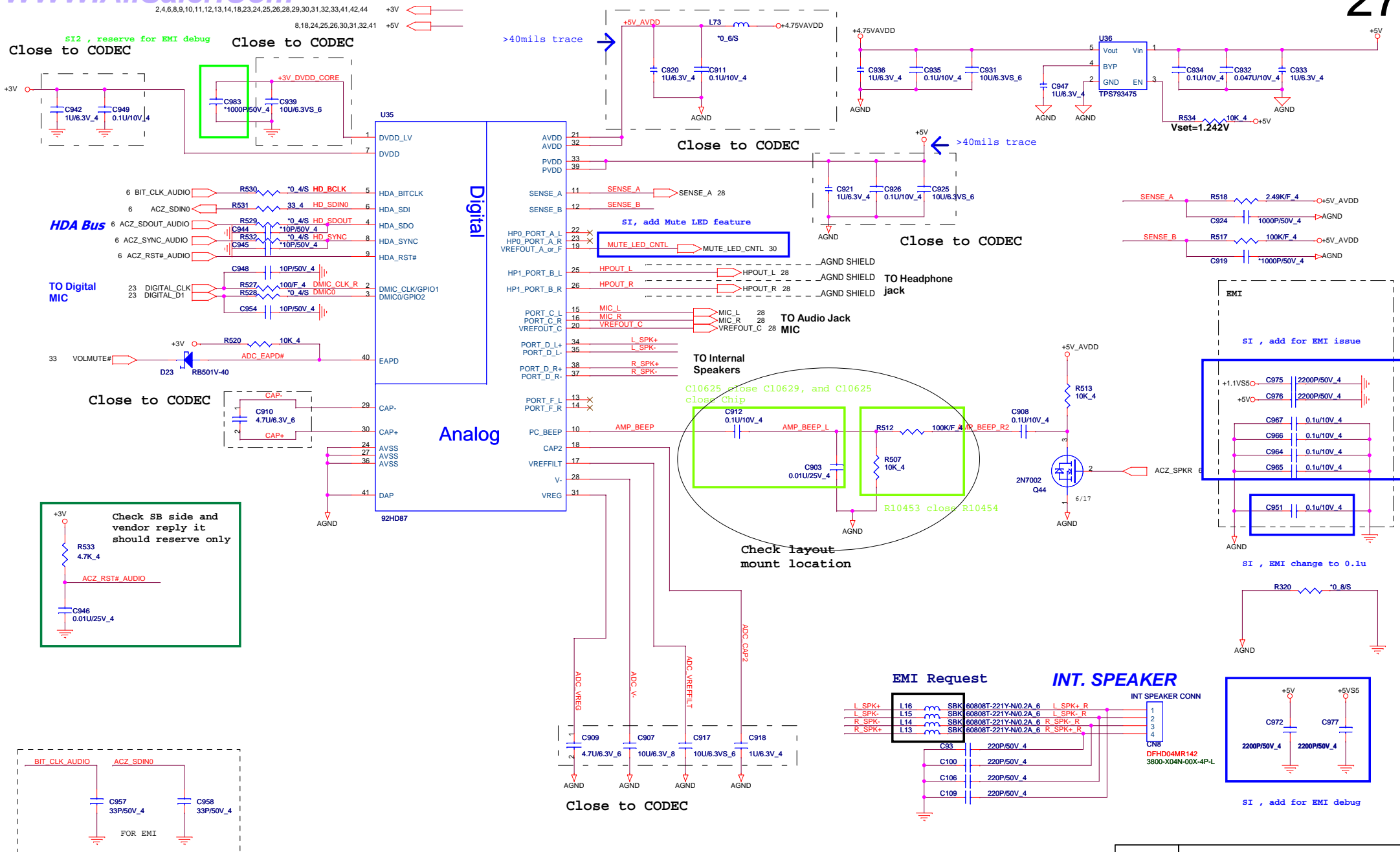
SI , EMI reserve for debug

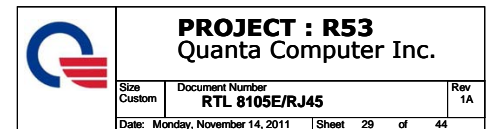


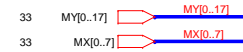
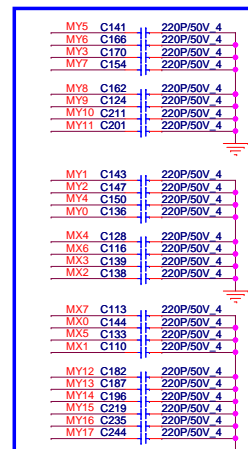
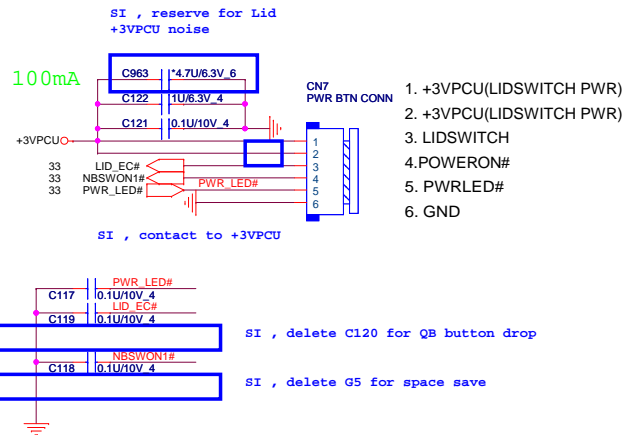
SI, add C981 for EMI issue

SD / MMC CARD READER CN12

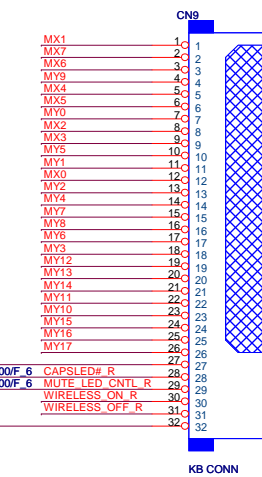
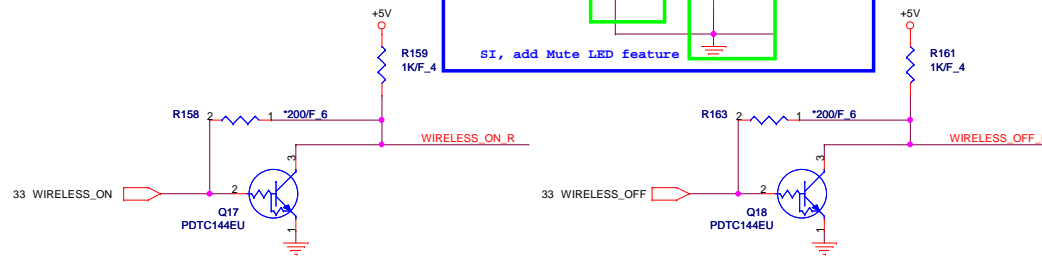
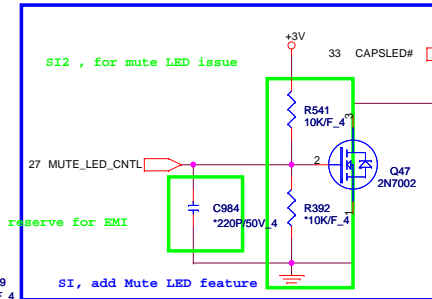




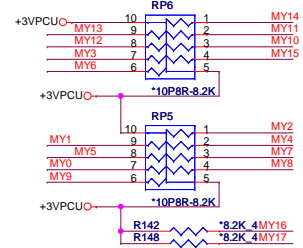




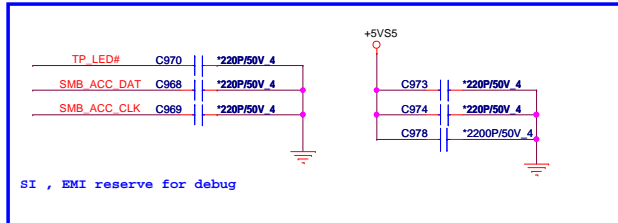
SI , mount for EMI



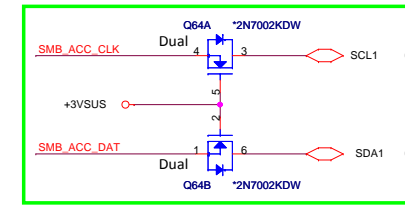
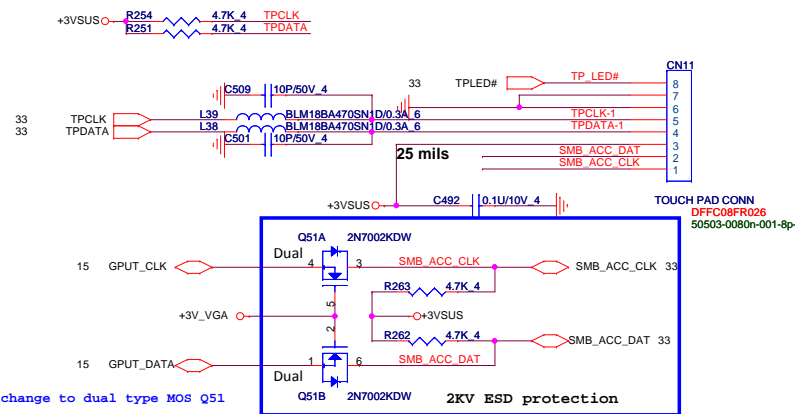
KEYBOARD PULL-UP



TOUCH PAD Con.



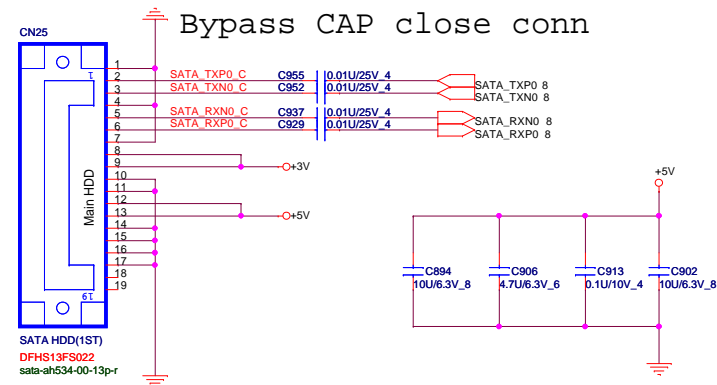
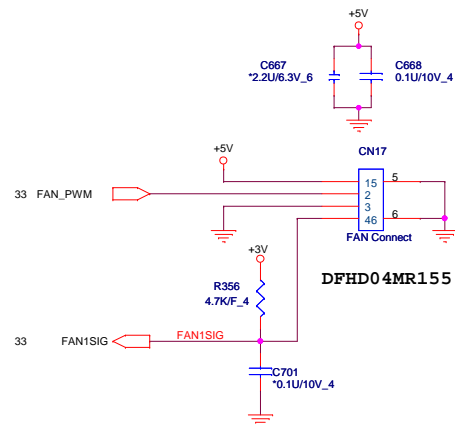
change to +3VSUS
close conn



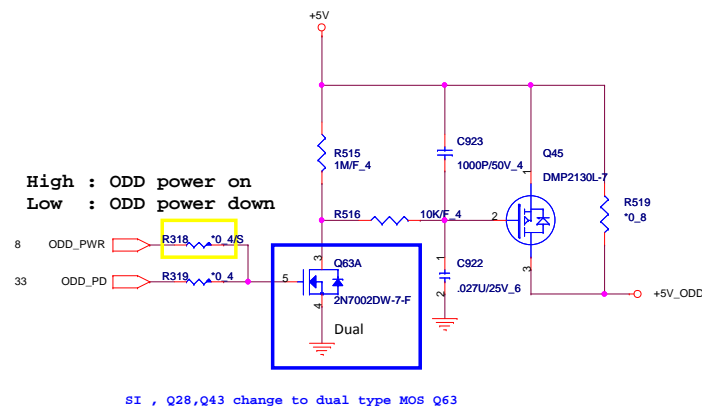
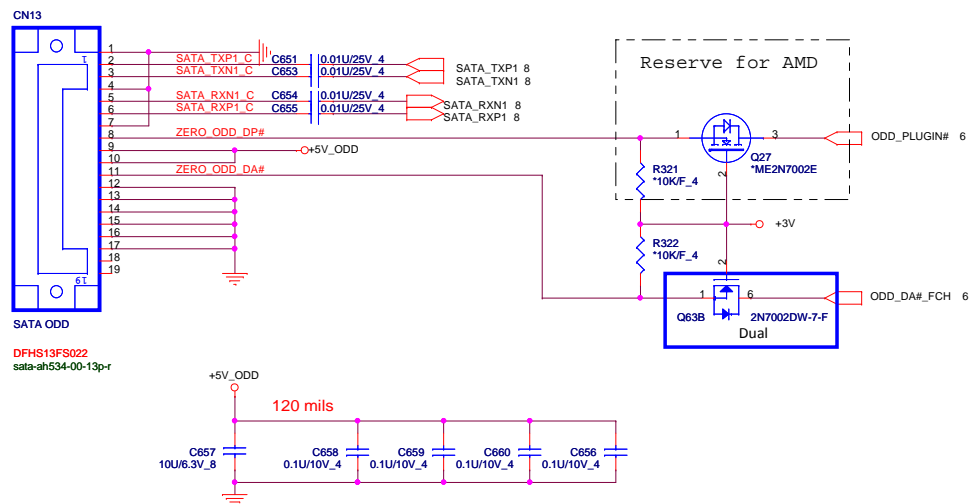
SI2 , HP request Image sensor
SMBUS reserve to FCH

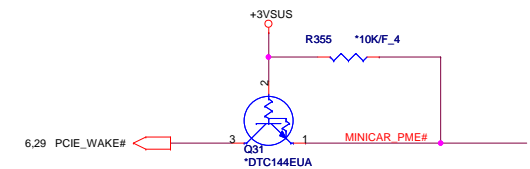
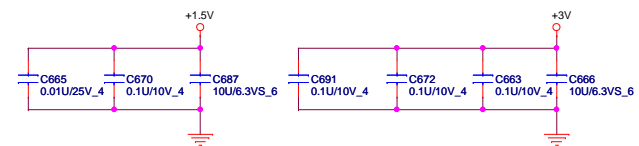
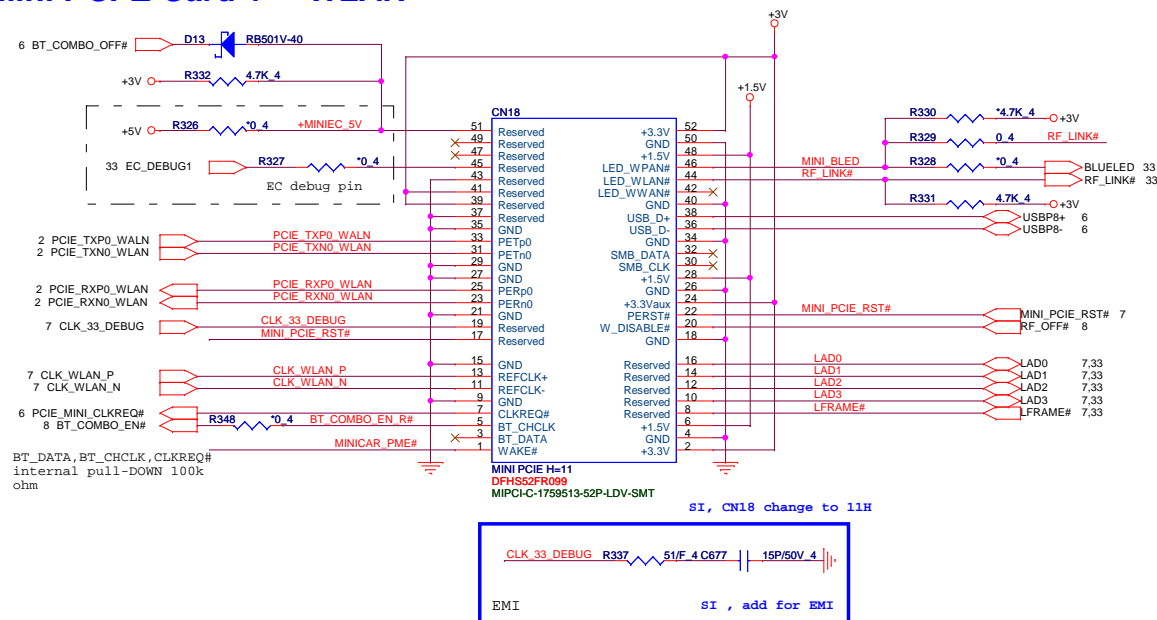
SI , Q21,Q22 change to dual type MOS Q51

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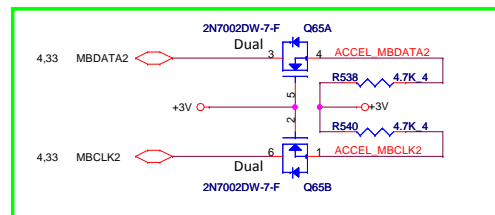


SATA ODD CONNECTOR SATA ODD

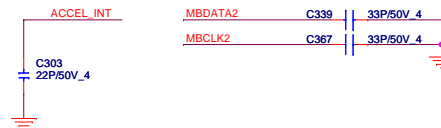
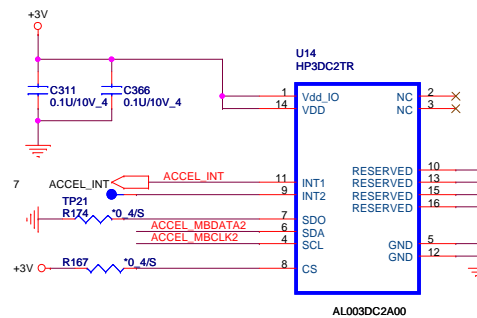





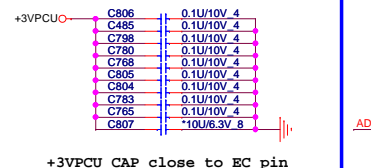
Accelerometer Sensor



SI2 , add for avoid leakage
from SUS power



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[illegible]

Change to 1S3355 as Current loss

D18
1S3355

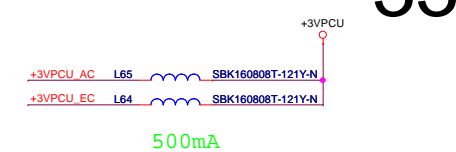
AD_TYPE R387 10K/F 4

R383 100/F 4 AD_ID 34

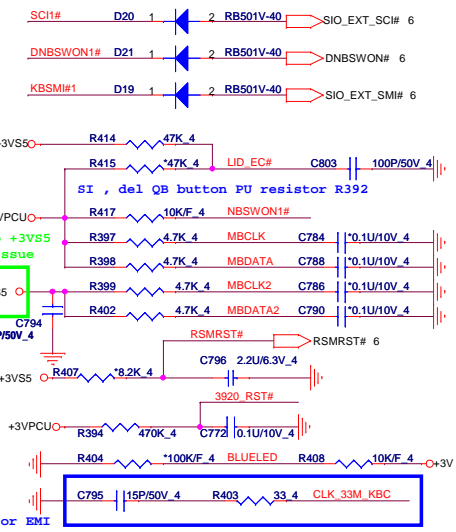
C739 0.1U/10V 4

R382 12K/F 4

C737 100P/50V 4



Change to RB500 as Current loss

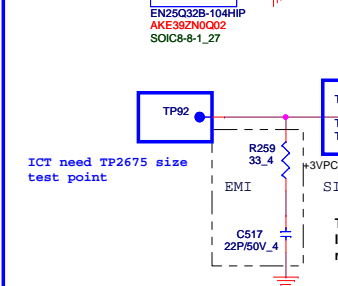


Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

The diagram shows the U20 chip with the following connections:

- BIOS_CS# (pin 1) connected to a red line.
- BIOS_SPI_CLK_I (pin 6) connected to a red line.
- BIOS_WR# (pin 5) connected to a red line.
- BIOS_RD# (pin 2) connected to a red line.
- SPI_3P (pin 3) connected to a red line.
- CE# (pin 8) connected to VDD.
- SCK (pin 9) connected to a red line.
- SI (pin 7) connected to a red line labeled SPI 7P.
- SO (pin 10) connected to a red line.
- HOLD# (pin 11) connected to a red line.
- WP# (pin 4) connected to a red line.
- VSS (pin 12) connected to ground.

Chip information: EN25Q32B-104HIP, AKE39ZN0Q02, SOIC8-1_27

[illegible]

+3VPCUO R395 10K/F 4 GPIO42 R396 *10K/F 4

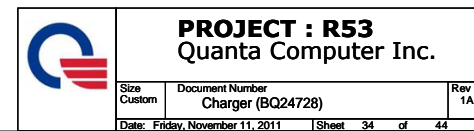
Hi ==> DIS/SG
Low ==>UMA

Platform model	GPI042	adapter
SG/DIS	High	90W
UMA	Low	65W



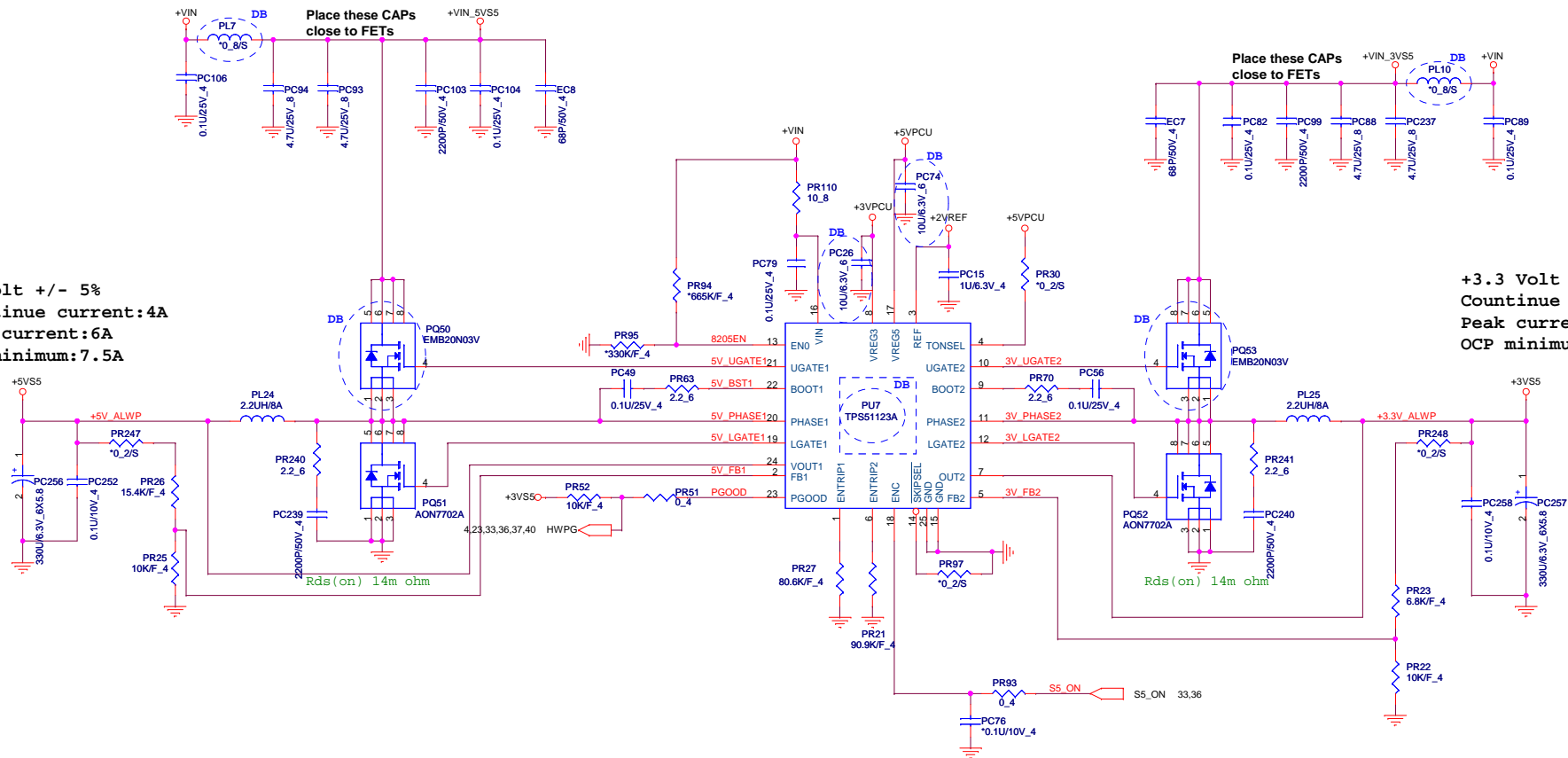
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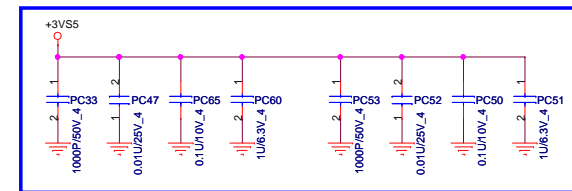



+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

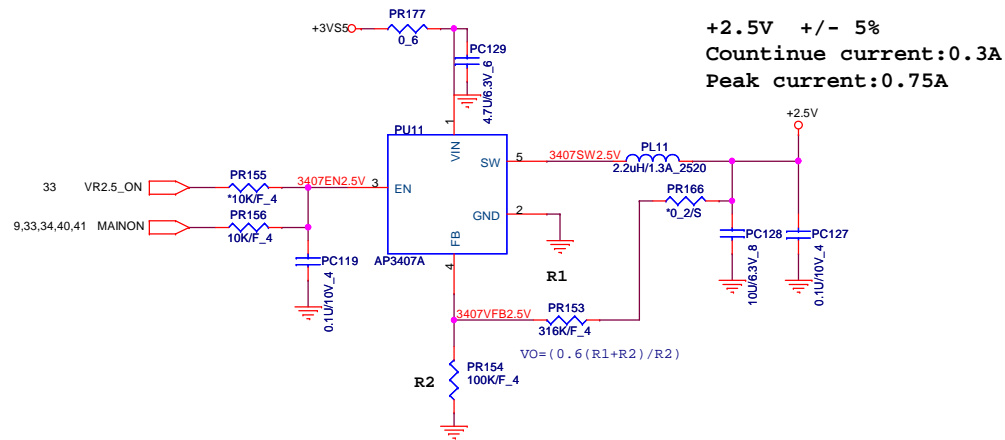
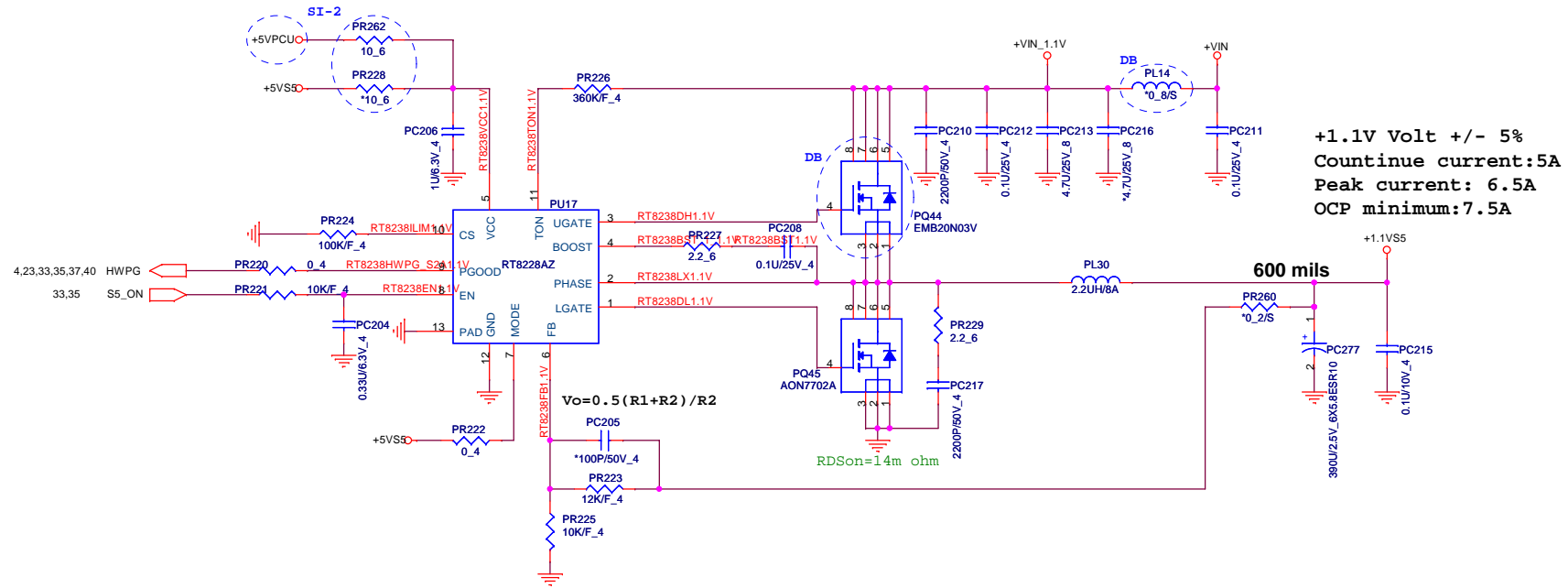
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

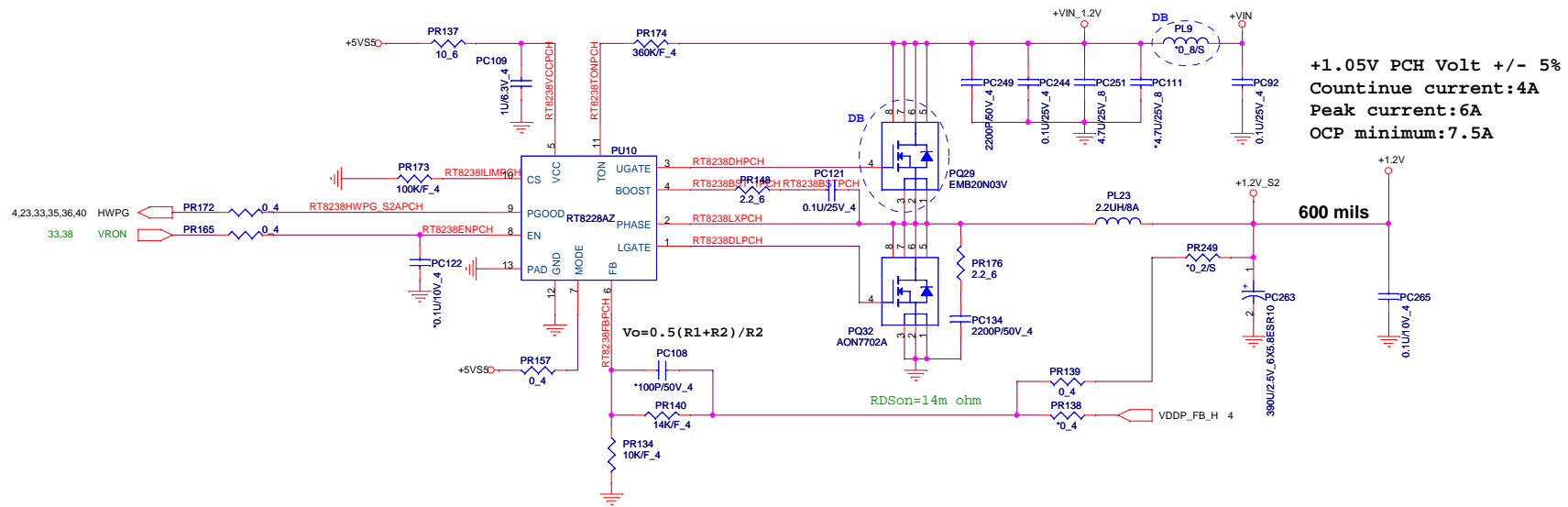


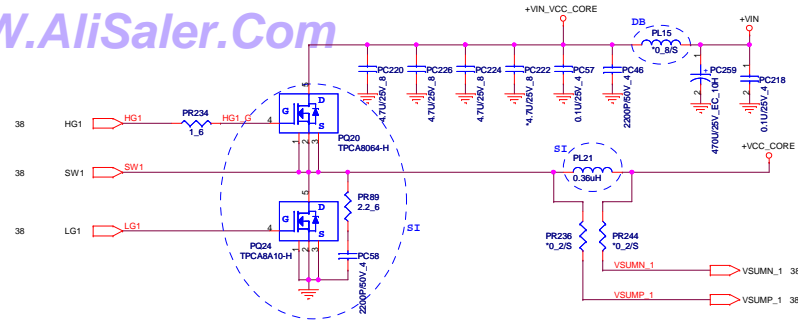
DB for prevent interference



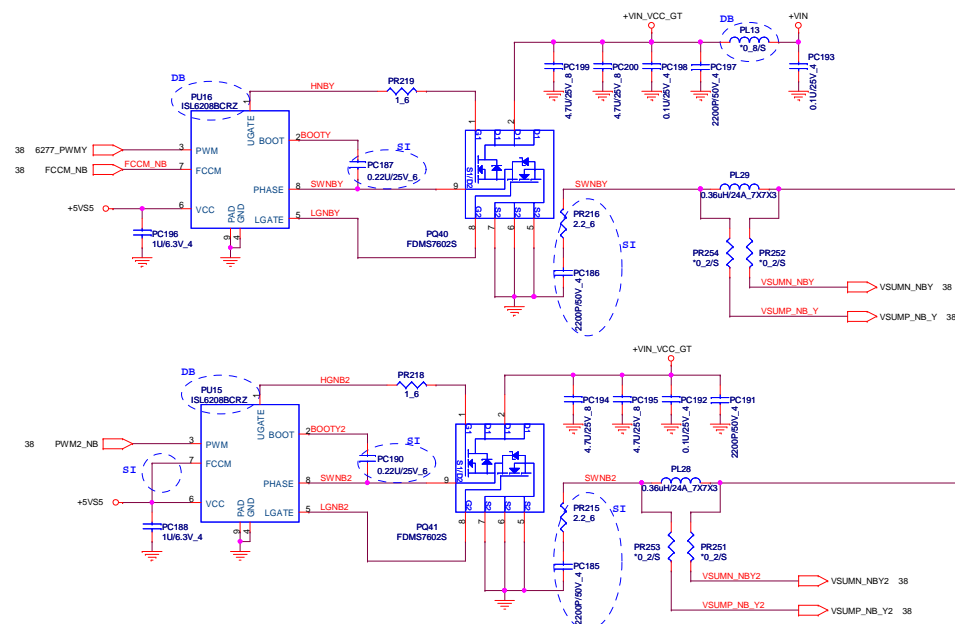
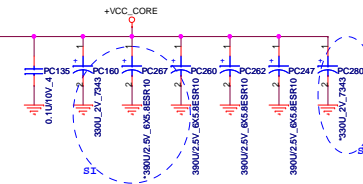
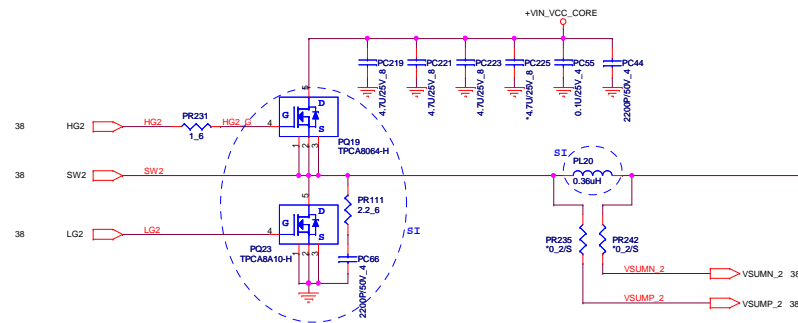
 PROJECT : R53 Quanta Computer Inc.		
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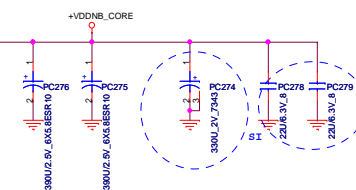


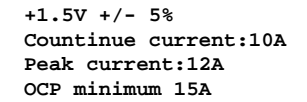


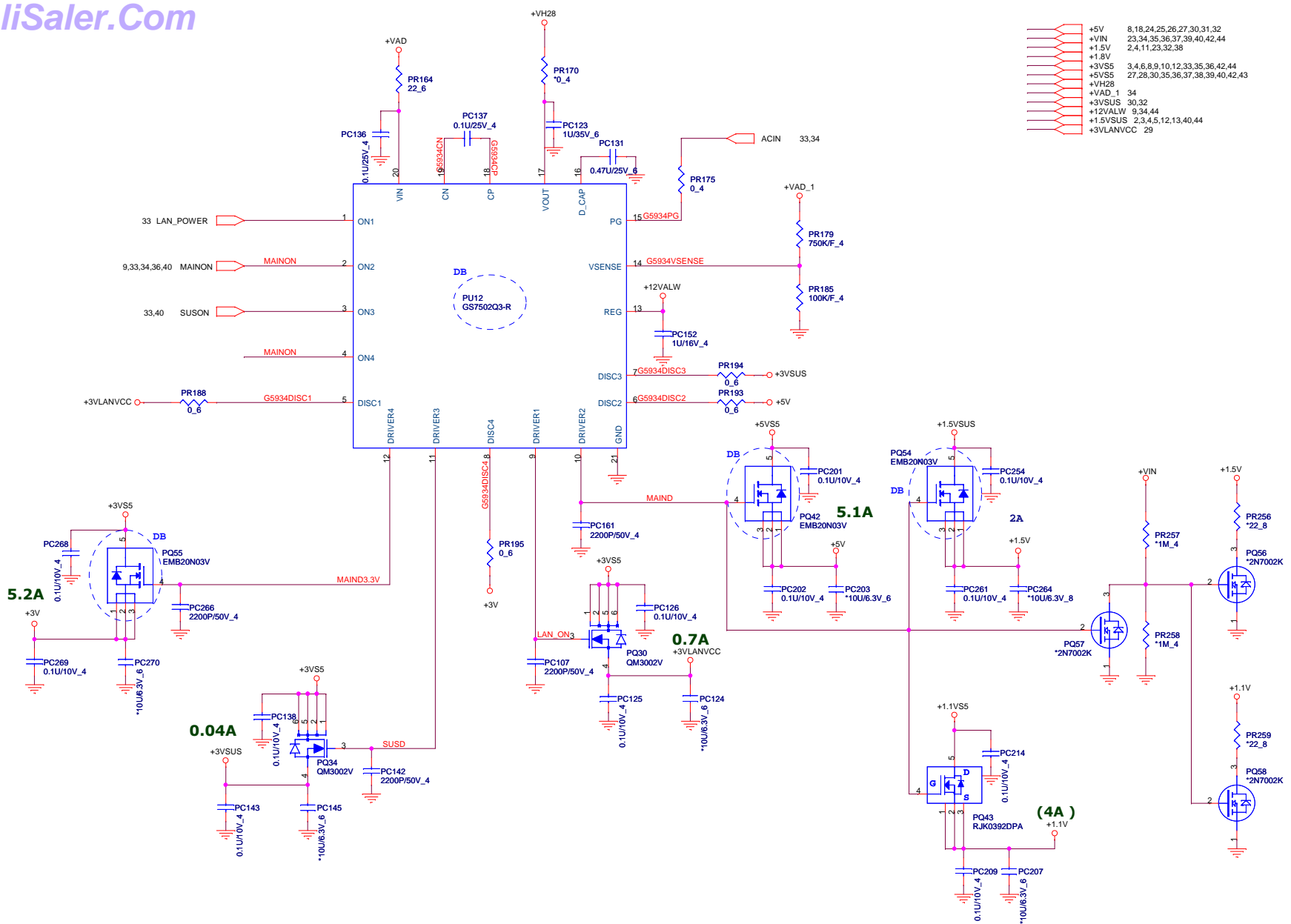
CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:60A




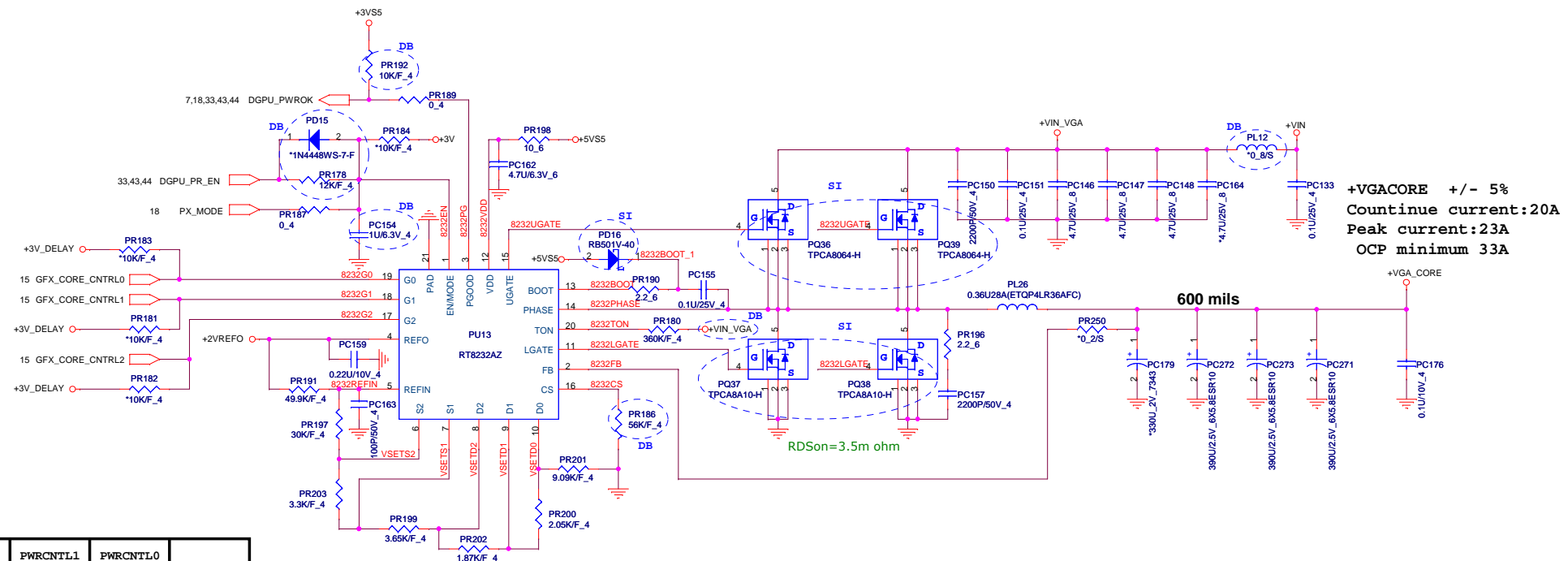
VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A








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Symour-XT	PWRCNTL2 (GPIO16)	PWRCNTL1 (GPIO20)	PWRCNTL0 (GPIO15)	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V



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